PRELIMINARY

2147A
HIGH SPEED 4096 x 1 BIT STATIC RAM

	2147A-3	2147AL-3	2147A	2147AL
Max. Access Time (ns)	55	55	70	70
Max. Active Current (mA)	50	35	50	35
Max. Standby Current (mA)	20	12	20	10

- Pinout and Functionally Compatible with the Industry Standard 2147H and the 6147
- Low Power Operation - 275 mW Maximum
- Lower Input/Output Leakage Current
- 0.8-2.0V Output Timing Reference Level
- Automatic Power Down Mode
- High Density 18-Pin Plastic/Cerdip Package
- Advanced HMOS-II Technology
- Directly TTL Compatible—All Inputs and Outputs
- Improved Output Current Drive
- Three-State Output for Bus Interface

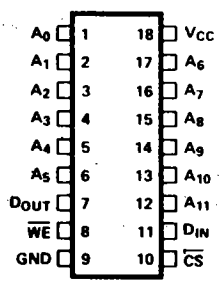
The Intel 2147A is a 4096 words by 1 bit static RAM designed for low power dissipation of 275 mW maximum. The 2147A is fully compatible with the industry standard 2147H and is fabricated on Advanced HMOS-II, an evolution of HMOS-II technology - a production proven process for high reliability, high performance, and high storage density.

The 2147A is fully static which results in reduced overhead costs by elimination of refresh clocking circuitry and by simplification of timing requirements. When deselected, the 2147A automatically changes into a low power standby mode and maintains this state until the chip select signal, CS, is low.

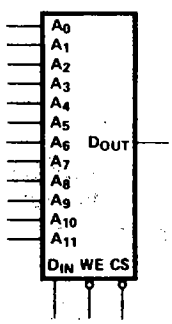
Accordingly, the 2147A is suitable for use in applications such as instrumentation, telecommunications, caches, writeable control store, fast buffer memories and large memory systems in which a majority of units are deselected.

The 2147A is placed in an 18 pin plastic or cerdip package and is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three state output are used.

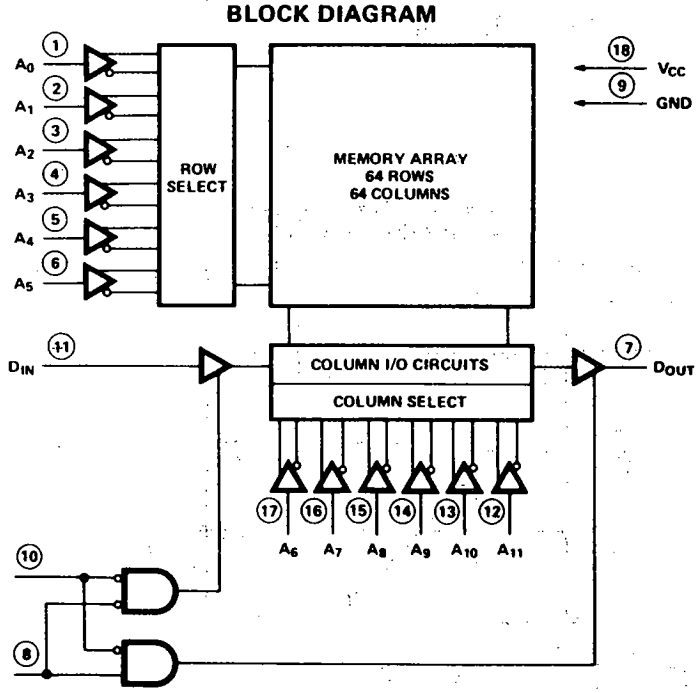
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

($T_A = 0°C$ to 70°C, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.)

Symbol	Parameter	2147A-3 Min.	2147A-3 Typ.	2147A-3 Max.	2147AL-3 Min.	2147AL-3 Typ.	2147AL-3 Max.	2147A Min.	2147A Typ.[2]	2147A Max.	2147AL Min.	2147AL Typ.[2]	2147AL Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current (All Input Pins)			1			1			1			1	μA	V_{CC} = Max., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10			10			10			10	μA	$\overline{CS} = V_{IH}$, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current			50			35			50			35	mA	V_{CC} = Max., $\overline{CS} = V_{IL}$, Outputs Open
I_{SB}	Standby Current			20			12			20			10	mA	V_{CC} = Min. to Max., $\overline{CS} = V_{IH}$
I_{PO}[3]	Peak Power-On Current			18			18			18			18	mA	V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-3.0		0.8	-3.0		0.8	-3.0		0.8	-3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4			0.4	V	I_{OL} = 12 mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			2.4			V	I_{OH} = −8 mA
$\|I_{OS}\|$[4]	Output Short Circuit Current			275			275			275			275	mA	V_{OUT} = GND to V_{CC}

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are
   θ_{JA} (@ 400 f_{PM} air flow) = 40° C/W
   θ_{JA} (still air) = 70° C/W
   θ_{JC} = 25° C/W
2. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$, and specified loading.
3. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
4. Duration not to exceed 1 sec.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	0.8-2.0V
Output Load	See Figure 1

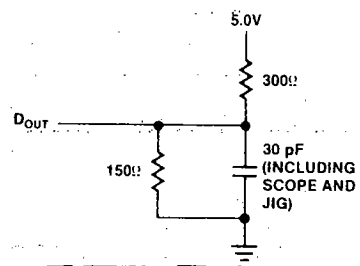


Figure 1. Output Load

CAPACITANCE[5] ($T_A = 25°C$, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	6	pF	$V_{OUT} = 0V$

NOTE:
5. This parameter is sampled and not 100% tested.

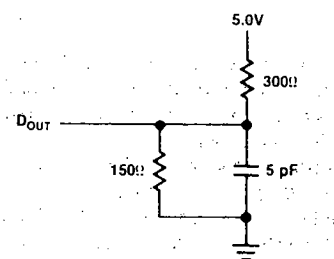


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

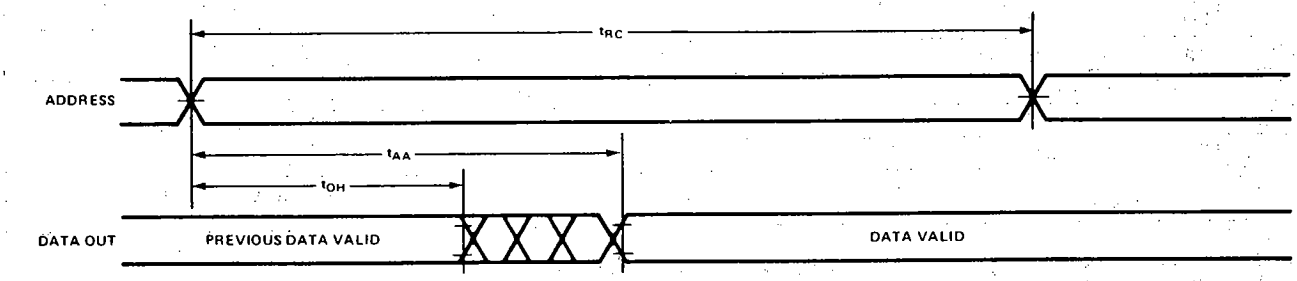
A.C. CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.)

Read Cycle

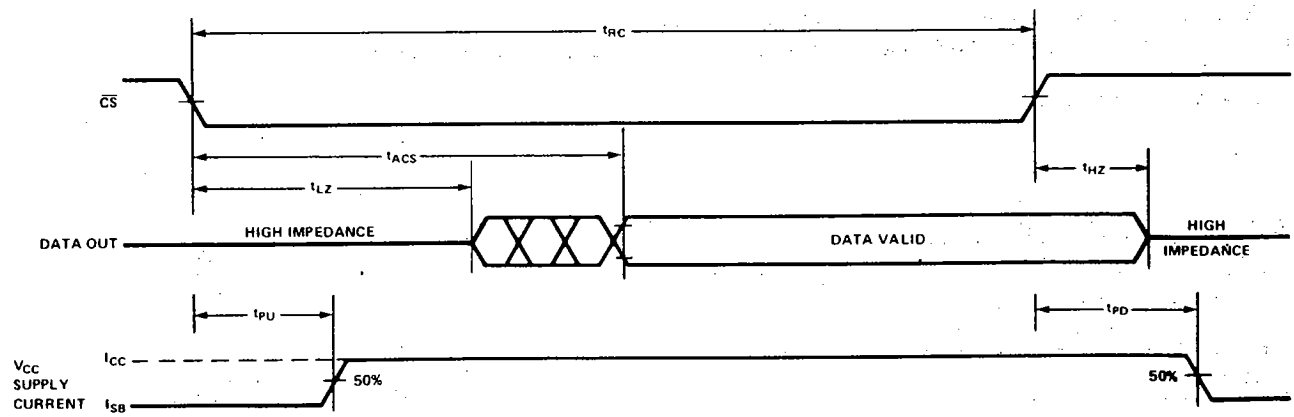
Symbol	Parameter	2147A-3, 2147AL-3 Min.	2147A-3, 2147AL-3 Max.	2147A, 2147AL Min.	2147A, 2147AL Max.	Unit
t_{RC} [1]	Read Cycle Time	55		70		ns
t_{AA}	Address Access Time		55		70	ns
t_{ACS1} [8]	Chip Select Access Time		55		70	ns
t_{ACS2} [9]	Chip Select Access Time		65		80	ns
t_{OH}	Output Hold from Address Change	5		5		ns
t_{LZ} [2,3,7]	Chip Selection to Output in Low Z	10		10		ns
t_{HZ} [2,3,7]	Chip Deselection to Output in High Z	0	30	0	40	ns
t_{PU}	Chip Selection to Power Up Time	0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		30	ns

WAVEFORMS

Read Cycle No. 1 [4,5]



Read Cycle No. 2 [4,6]



NOTES:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1. Applies to 2147A, 2147AL, 2147A-3, and 2147AL-3.

A.C. CHARACTERISTICS (Continued)

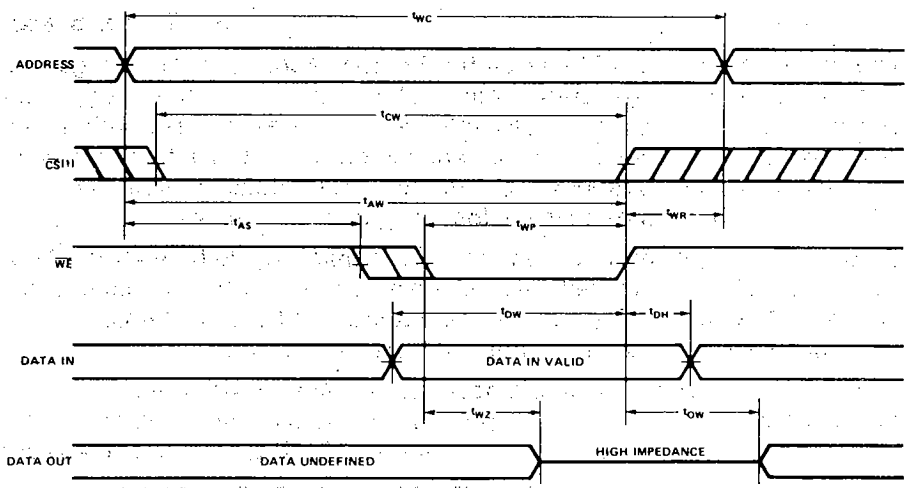
Write Cycle

Symbol	Parameter	2147A-3, 2147AL-3 Min.	2147A-3, 2147AL-3 Max.	2147A, 2147AL Min.	2147A, 2147AL Max.	Unit
t_{WC} [2]	Write Cycle Time	55		70		ns
t_{CW}	Chip Selection to End of Write	45		55		ns
t_{AW}	Address Valid to End of Write	45		55		ns
t_{AS}	Address Setup Time	0		0		ns
t_{WP}	Write Pulse Width	35		40		ns
t_{WR}	Write Recovery Time	10		15		ns
t_{DW}	Data Valid to End of Write	25		30		ns
t_{DH}	Data Hold Time	10		10		ns
t_{WZ} [3]	Write Enabled to Output in High Z	0	25	0	35	ns
t_{OW} [3]	Output Active from End of Write	0		0		ns

WAVEFORMS

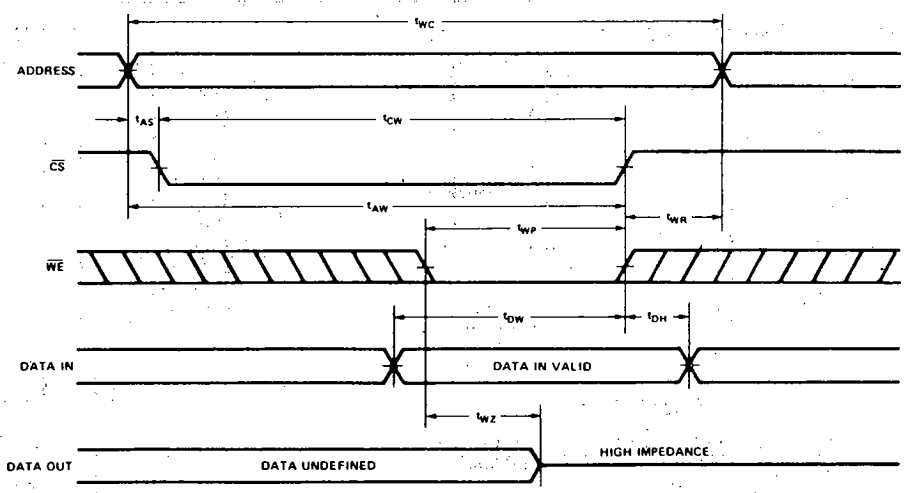
Write Cycle No. 1

($\overline{WE}$ CONTROLLED)[4]



Write Cycle No. 2

($\overline{CS}$ CONTROLLED)[4]



NOTES:

1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.